

Claims

- [c1] An integrated circuit comprising:
a plurality of memory banks;
a plurality of comparator units, a comparator unit being coupled to a memory bank for comparing a test pattern written to the memory bank against data read from the memory bank; and
a BIST control unit coupled to the plurality of comparator units for testing the plurality of memory banks simultaneously, the BIST control unit provides test control signals and the test pattern to the comparator units.
- [c2] The integrated circuit of claim 1 wherein the test control signals comprise addresses of memory words to be tested.
- [c3] The integrated circuit of claim 2 wherein the memory banks occupy a common address space.
- [c4] The integrated circuit of claim 3 wherein the BIST control unit selects the banks simultaneously.
- [c5] The integrated circuit of claim 4 wherein the BIST control unit generates addresses in the common address space.
- [c6] The integrated circuit of claim 5 wherein the memory banks have different sizes.
- [c7] ✓ The integrated circuit of claim 1 wherein the comparator unit stores addresses of faulty cells.
- [c8] The integrated circuit of claim 7 wherein the faulty memory cells are replaced with redundant cells.
- [c9] The integrated circuit of claim 1 wherein the BIST control unit receives test results from the comparator units.
- [c10] The integrated circuit of claim 9 wherein the BIST control unit outputs the test results serially in response to an input clock signal.

- [c11] The integrated circuit of claim 10 wherein the test results comprise addresses faulty words.
- [c12] The integrated circuit of claim 11 wherein the test results further comprise locations of faulty bits within the faulty words.
- [c13] The integrated circuit of claim 1 wherein the memory bank comprises at least one memory sub-array.
- [c14] The integrated circuit of claim 13 wherein the memory sub-array comprises a plurality of memory cells.
- [c15] The integrated circuit of claim 14 wherein the memory cell comprises a first port and a second port.
- [c16] The integrated circuit of claim 15 wherein first bit lines and second bit lines interconnect the memory cells in a first direction.
- [c17] The integrated circuit of claim 16 wherein first word lines and second word lines interconnect the memory cells in a second direction.
- [c18] The integrated circuit of claim 17 wherein memory access is performed through the first port.
- [c19] The integrated circuit of claim 18 wherein refresh is performed through the second port.
- [c20] The integrated circuit of claim 19 wherein memory access is performed through the second port.
- [c21] The integrated circuit of claim 1 wherein the comparator unit comprises a test control unit and a testing circuit.
- [c22] The integrated circuit of claim 21 wherein the test control unit is coupled to an access control circuit and a refresh control unit.
- [c23] The integrated circuit of claim 1 wherein the testing comprises single-port testing.

[c24] The integrated circuit of claim 23 wherein the testing further comprises dual-port testing.